clock signal C_{out} by mixing the clock signals C0 to C3. These four clock signals C0 to C3 are shown in Fig. 5. The circuit contains two mixers, which are respectively operated with the appropriate clock phases and operate differentially on the same load resistors R1 and R2. A capacitor C1 (optional) is used for band-limiting, since only the fundamentals of the individual phases of the clock signals C1 to C3 need to be mixed (added), and harmonics need to be filtered out accordingly. The control voltages U0 to U4 are used to weight the respective clock signals C0 to C3 in an appropriate manner. --

A1 cont

In the Claims:

Please cancel claims 15-17.

Claim 11 (amended). A control loop, comprising:

A2 a phase shifter for producing an output with a first clock phase;

a phase detector for detecting a phase difference between a second clock phase of a data signal and the first clock phase, said phase detector producing an output signal based on the detected phase difference;

a charge pump for integrating the output signal of said phase detector, said charge pump producing a regulation signal for said phase shifter; and

said phase shifter changing over a phase regulation direction at predetermined switching points based on said regulation signal;

said changing over of said phase regulation direction being performed with a hysteresis behavior.

Claim 12 (amended). The control loop according to claim 11, in combination with a delay locked loop circuit, said delay locked loop circuit having a delay locked loop control loop including said phase shifter, said phase detector, and said charge pump.

G2 cont.

Claim 13 (amended). A method for producing a clock signal, which comprises:

detecting a phase difference between a clock phase of a first input signal and a clock phase of a first output signal of the phase shifter;

producing a second output signal based on the detected phase difference;

producing a second input signal for the phase shifter by integrating the second output signal; and

changing a phase regulation direction of the phase shifter at predetermined switching points based on the second input signal, the changing over of the phase regulation direction being performed with a hysteresis behavior.

Claim 14 (amended). A phase shifter for producing an output signal, which comprises:

a circuit for receiving an input signal having a phase;

G2 cont-

said circuit also for producing an output signal having a phase;

the output signal selected from the group consisting of a proportional signal essentially proportional to the phase of the input signal and an inversely proportional signal essentially inversely proportional to the phase of the input signal;

said circuit being designed such that the output signal changes between the proportional signal and the inversely

proportional signal at predetermined switching points based on the input signal of said charge pump.